Patent claims

1. An integrated test circuit arrangement (10) having integrated test structures (80 to 86),

and having at least one of the following elements or units:

at least one integrated heating element (70)

and/or an integrated detection unit (102, 42), which detects at least one physical property in each case for the test structures (80 to 86),

and/or having an integrated supply unit, which supplies the test structures with a current or a voltage in each case in switchable fashion independently of one another.

2. The circuit arrangement (10) as claimed in claim 1, characterized by more than fifty or more than one hundred or more than one thousand test structures.

3. The circuit arrangement (10) as claimed in claim 1 or 2, characterized in that test structures (80 to 86) of a group (T1) have the same construction among one another,

and/or in that the test structures (80 to 86) of a group are or contain interconnects which preferably contain a metal or comprise a metal and/or which are led into another metallization layer by means of a via or contact hole,

and/or in that the test structures of a group (T2) are or contain dielectrics,

and/or in that the test structures of a group (T3) are

or contain active or passive electronic components, in particular transistors, capacitors, resistors or coils,

and/or in that the test structures of different groups are integrated in the circuit arrangement (10), preferably spatially, in particularly in different planes parallel to the plane of a carrier substrate for the test structures (T1 to T5),

and/or in that a group (T1 to T5) contains more than fifty or more than one hundred or more than one thousand test structures.

4. The circuit arrangement (10) as claimed in one of the preceding claims, characterized by a supply unit (40, 40a), which feeds the test structures (80 to 86) with a current or a voltage in each case in switchable fashion preferably independently of one another,

and/or the supply unit containing a multiplicity of integrated current sources (60 to 68) and/or a multiplicity of integrated voltage sources,

and/or the current sources (60 to 68) containing a plurality of current mirrors which in each case generate a multiple or a fraction of a reference current or a current having the magnitude of the reference current.

5. The circuit arrangement (10) as claimed in one of the preceding claims, characterized in that the heating element (70) contains a resistance heating element which preferably contains monocrystalline silicon or polycrystalline silicon or comprises monocrystalline silicon or polycrystalline silicon or which contains a metal or comprises a metal, the silicon preferably being doped,

and/or in that the heating element (70) has a straight profile, a meandering profile, a triangular function profile or a rectangular function profile.

6. The circuit arrangement (10) as claimed in one of the preceding claims, characterized by at least one reference structure (88), the construction and/or the dimensions of which differ from the construction and/or the dimensions of a test structure (80 to 86).

7. The circuit arrangement (10) as claimed in one of the preceding claims, characterized in that the detection unit is connected or can be connected to the test structures (80 to 86),

and/or in that the detection unit contains at least one counter unit (36), which is clocked in accordance with a predetermined clock (T).

8. The circuit arrangement (10) as claimed in one of the preceding claims, characterized in that the detection unit contains at least one multiplexer unit (102), the inputs of which are electrically connected to a respective test structure (80 to 86),

and/or in that the output of the multiplexer unit (102) is connected to the input of a comparison unit (42a), the other input of which is electrically connected to a reference structure (88), the reference structure (88) having a different construction and/or different dimensions than a test structure (80 to 86).

9. The circuit arrangement (10) as claimed in one of the preceding claims, characterized by a control unit (34), which is connected to the outputs of the detection unit on the input side and which outputs detection results and/or which controls the supply unit in a manner dependent on the detection results and/or

which outputs a datum for ascertaining the detection instant and/or which outputs a datum for identifying a test structure.

10. The circuit arrangement (10) as claimed in one of the preceding claims, characterized by a substrate,

the test structures (T1 to T5) and/or the heating element (70) and/or the supply unit (40) and/or the detection unit (42) and/or the control unit (34) in each case being arranged in the substrate and/or mechanically fixedly on the substrate.

11. The circuit arrangement (10) as claimed in one of the preceding claims, characterized in that the circuit arrangement (10) contains electronic components associated with a user circuit, in particular with a memory unit and/or with a processor.

12. The circuit arrangement (10) as claimed in one of the preceding claims, characterized in that the circuit arrangement (10) is encapsulated in a plastic housing or in a ceramic housing.

13. A method for testing test structures (80 to 86), in particular with a circuit arrangement (10) as claimed in one of the preceding claims,

having the following steps that are implemented without limitation by the order specified:

integration of test structures (80 to 86) into an integrated circuit arrangement (10),

integration of a detection unit (102, 42), which detects at least one physical property for the test structure,

integration of at least a part of a supply unit (60 to 68) into the integrated circuit arrangement (10),

connection of the test structures (80 to 86) to the supply unit (60 to 68) or to a supply unit,

detection in each case of a physical property of the test structures (80 to 86) by means of the detection unit (102, 42) or by means of a detection unit.

14. The method as claimed in claim 13, characterized by the following steps:

integration of at least one heating element (70) into the integrated circuit arrangement (10),

warming or heating of the test structures (80 to 86) with the aid of the heating element (70),

and/or the supply unit (60 to 68) being connected to the test structure during warming or during heating.

15. A method for testing test structures (80 to 86), in particular with a circuit arrangement (10) as claimed in one of the preceding claims,

having the following steps that are implemented without limitation by the order specified:

integration of test structures (80 to 86) into an integrated circuit arrangement (10),

integration of at least one heating element (70) into the integrated circuit arrangement (10),

warming or heating of the test structures (80 to 86) with the aid of the heating element (70),

connection of the test structures (80 to 86) to at least one supply unit (60 to 68),

detection in each case of a physical property of the test structures (80 to 86).

16. The method as claimed in one of claims 13 to 15, characterized in that the physical property relates to the reliability.

17. The method as claimed in one of claims 13 to 16, characterized by the following steps:

integration of at least one reference structure (88), the construction and/or the dimensions of which differ from the construction and/or the dimensions of a test structure (80 to 86),

detection of a physical reference property at the reference structure (88),

comparison of the physical property of a test structure (80 to 86) with the reference property or comparison of a quantity generated from a physical property and a quantity generated from the reference property,

and/or registering of an instant at which the comparison result changes.

18. The method as claimed in one of claims 13 to 17, characterized in that preferably the same the physical properties of different test structures (80 to 86) are successively compared with a reference property.

19. The method as claimed in one of claims 13 to 18, characterized in that the heating element (70) is fed with an AC current and/or a DC current,

and/or in that the heating element (70) is heated to temperatures of greater than two hundred degrees Celsius or greater than three hundred degrees Celsius.

20. The method as claimed in one of claims 13 to 19, characterized in that an output circuit (34) is integrated into the integrated circuit arrangement (10), which output circuit outputs at least one set of detection data for the test structures (80 to 86).

21. The method as claimed in one of claims 13 to 20, characterized in that it is implemented with an unencapsulated integrated circuit arrangement (10), in particular with an integrated circuit arrangement (10) that has not yet been incorporated into a housing, and/or with an integrated circuit arrangement (10) that is still arranged on a semiconductor wafer, the semiconductor wafer preferably carrying a multiplicity of other integrated circuit arrangements,

and/or in that the method is implemented for the purpose of monitoring ongoing production.

22. The method as claimed in one of claims 13 to 21, characterized by the following step:

integration of at least a part of the supply unit (60 to 68) into the integrated circuit arrangement (10), said part containing at least one active component, preferably a transistor.